A hybrid multilevel inverter topology for drive applications

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***Abstract* - Use of multilevel inverters is becoming popular in the recent years for high power applications. Various topologies and modulation strategies have been reported for utility and drive applications in the recent literature. This paper is devoted to the investigation of a 500 HP induction machine drive based on a seven-level 4.5 kV hybrid inverter. The topological structure and operating principles of the proposed approach are presented. Various design criteria, spectral structure and other practical issues such as capacitor voltage balancing are discussed. The feasibility of the proposed approach is verified by computer simulations.**

I. INTRODUCTION

Multilevel power conversion has been receiving increasing attention in the past few years for high power applications [1], [2]. Numerous topologies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating.

The early interest in multilevel power conversion technology was perhaps triggered by Nabae et al. [3] who introduced a neutral point clamped topology. The resultant three-level waveform has considerably better spectral performance compared to that of the conventional voltage source inverter. The improvement in the spectral structure of output waveforms in using multiple levels was reiterated by Bhagwat and Stefanovic [4]. Subsequently, the original neutral point clamped topology has been extended to higher number of levels using the similar principle of clamping the intermittent levels with diodes [5]. In addition to improving the waveform quality, these multilevel inverters substantially reduce voltage stress on the devices. Such multilevel inverters are generically known as diode clamped inverters. However, in this type of inverters, the required voltage blocking capability of the clamping diodes varies with the levels. This may result in the requirement of multiple diodes at higher levels. So an alternative multilevel structure where the voltage across an open switch is constrained by clamping capacitors instead of clamping diodes has been proposed by Meynard [6]. These inverters are commonly known as flying capacitor inverters. Using multiple single level inverters to synthesize multilevel waveforms was initially realized through phase shifting of multiple single level converter output voltage waveforms and adding them vectorially using series connected transformer windings [7]. However when the number of levels increases beyond three or five, this approach becomes difficult to realize due to the requirement of multiple transformer windings. As an alternative method, a series connection of single phase inverters with multiple dedicated buses to realize multilevel waveforms was probably first presented in [8]. This modular approach has been investigated for utility applications [9], [10].

Recent trends in the power semiconductor technology indicate a trade-off in the selection of power devices in terms of switching frequency and voltage sustaining capability [11]. Normally, the voltage blocking capability of faster devices such as Insulated Gate Bipolar Transistors (IGBT) and the switching speed of high voltage devices like Gate Turn-Off (GTO) thyristors is found to be limited. With the aforementioned modular topologies, realization of the multilevel inverters using a hybrid approach involving GTO thyristors and IGBTs operating in synergism is possible.

This paper presents the investigation of a 500 HP induction machine drive based on a seven-level 4.5 kV hybrid inverter. The proposed topology is a combination of a GTO inverter with a 3 kV bus and a IGBT inverter with a 1.5 kV bus. Using appropriate modulation strategy, it will be possible to synthesize stepped waveforms with seven voltage levels viz. -4.5 kV, -3 kV, -1.5 kV, 0, 1.5 kV, 3 kV, 4.5 kV. In addition to this new concept, a hybrid modulation strategy which incorporates stepped synthesis in conjunction with variable pulse width of the consecutive steps is presented. Under this modulation strategy, while the GTO inverter will be modulated to switch only at fundamental frequency of the inverter output, the IGBT inverter will be used to switch at a higher frequency thereby providing additional improvements in the waveform quality. With the proposed hybrid topology, the effective spectral response of the output depends on the IGBT switching, while the overall voltage generation capability is decided by the voltage ratings of the GTO thyristors.

The following section of this paper presents a review of the multilevel inverter based drives reported in the

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literature. A brief description of the conventional structure of H-bridge multilevel inverter is included in Section III. A modified configuration of this topology with non-identical dc voltage sources is described in section IV. It is observed that the number of synthesized levels increases exponentially with a binary arrangement of dedicated dc voltage sources. Section V describes the proposed hybrid configuration for a 500 HP induction machine drive application. The topology and operating principles of this approach are discussed in this section. Simulation results verifying the efficacy of the proposed approach are given in Section VI. A summary of various results and a comparison of the proposed approach with the topologies reported in literature is presented in the concluding section.

II. Multilevel Inverter Based Drives

So far, interest in the multilevel power conversion has been largely restricted to utility applications such as static VAr compensation, active filtering etc [1]. However, this technology has been recently investigated for induction machine drive applications [12]-[14]. Menzies et al. have proposed a five-level GTO inverter for a 22 MVA induction machine drive [12]. A single phase of the diode clamped multilevel structure proposed in their paper is shown in Fig. 1. The remaining two phases have a similar switch-diode configuration and share the same dc bus. It may be observed from this figure that a five-level waveform can be synthesized at point A by tapping five points (A_1, A_2, A_3, A_4, A_5) on the quadruple dc bus. The circuit can be thought of as a multiplexer, attaching output to one of the five available voltage levels. All the capacitors are identical and the dc voltage levels are 2.65 kV each. So a peak voltage of ± 5.3 kV can be realized by clamping the phase output to the top (A_1) or bottom (A_5) of the dc bus. This can be done by closing a set of four switches viz. S_1-S_4 or S_5-S_8. The inner voltage levels 2.65 kV, 0, -2.65 kV can be synthesized by closing switches S_2-S_5 or S_3-S_6 or S_4-S_7 respectively. This creates a current path connecting two of the clamp diodes back-to-back. The other end of these back-to-back clamp diodes is connected to one of the voltage taps (A_2, A_3, A_4) along the dc bus. These diodes also prevent the undesired voltage level from getting connected to the output.

It has been demonstrated that the synthesis of 3 ϕ 7.46 kV line-line ac voltage is possible using 4.5 kV GTO thyristors with this topology. However, since the switching capability of the GTO thyristors is limited at higher frequencies, the spectral performance is hampered. The authors also demonstrate that the dc bus is loaded non-uniformly for an induction machine drive application thus causing a problem of capacitor voltage balancing.

Sinha and Lipo [13] have recently presented a four-level IGBT rectifier-inverter system for drive applications. A diode clamped structure is used on both rectifier and inverter ends. A single phase of the proposed topology is illustrated in Fig. 2. The operating principle of the four-level inverter is similar to that of the five-level inverter as discussed earlier. The four-level waveform is synthesized by a triple dc bus which allows four distinct levels. A set of three switches is closed at any given time which connects the output phase to one of these four levels.

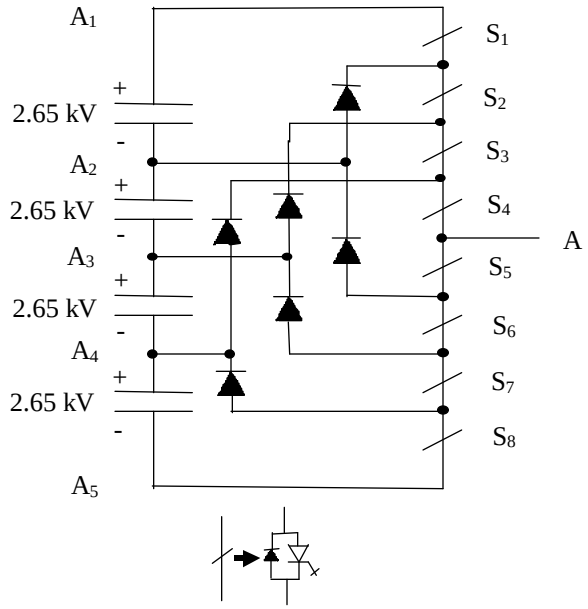

Fig. 1. Simplified schematic of a single phase of a five-level diode clamped inverter.

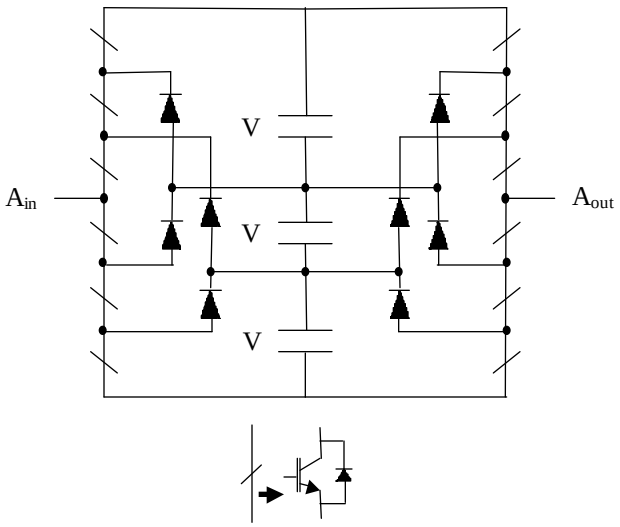

Fig. 2. Simplified schematic of a single phase of a four-level diode clamped rectifier- inverter.

In addition to the solution for capacitor voltage balancing, a control strategy to ensure a unity power factor on the utility side is also discussed. The authors propose to use IGBTs which offer better switching characteristics than the GTO thyristors. However, it is difficult to scale this approach to a higher voltage level owing to the upper bound on the IGBT voltage ratings. Moreover, the diode clamped topology of this converter makes it cumbersome and difficult to realize such an inverter beyond four-five levels.

III. H-Bridge Multilevel Inverter

References [9], [10], [14] have proposed a per phase power conversion scheme for synthesizing multilevel waveforms. The authors present a modular topology as illustrated in Fig. 3 to realize multilevel power conversion. In this approach, a number of full bridge single phase inverters with dedicated isolated dc bus capacitors/voltage sources are connected together in series to form a high voltage inverter for each phase of the system. Fig. 3 shows two such single phase inverters using IGBTs connected in series to form a single phase of the multilevel inverter. The remaining two phases have a similar switch configuration and respective independent dc voltage sources. It may be seen that the inverter is capable of synthesizing five distinct voltage levels (±2V, ±V, 0) if all the dc bus voltages are equal to 'V'.

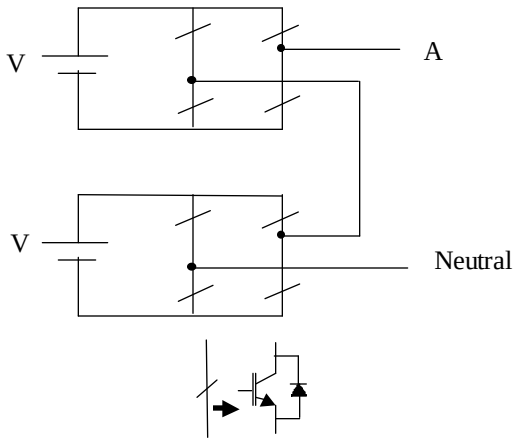

Fig. 3. Simplified schematic of a single phase of a five-level H-bridge inverter with two equal dc voltage levels.

The advantage of this topology is that it provides flexibility for expansion of the number of levels easily without introducing undue complexity in the power circuit. Moreover, it requires same number of switches as in a diode clamped topology to achieve a given number of (odd) voltage levels. However this configuration requires multiple dedicated dc buses which makes it an expensive solution. On the other hand, since the dc voltage sources are independent, the problem of capacitor voltage balancing is obviated.

IV. Modified H-Bridge Multilevel Inverter

As mentioned in the last section, an H-bridge multilevel inverter offers numerous advantages like modularity, least number of switches for a given number of levels, simple capacitor voltage balancing etc. As shown in Fig. 3, the reported topologies for H-bridge multilevel inverters have identical dc voltage levels. In general, such a multilevel inverter with 'n' equal dc voltage levels can offer 2n + 1 distinct voltage levels at the phase output. The performance attributes of the output waveform in terms of number of levels can be further enhanced by using unequal dc voltage levels. For instance, a set of cascaded inverters with dc voltages varying in binary fashion gives an exponential increase in the number of levels. For 'n' such cascaded inverters, with dc voltage levels varying in binary fashion, one can achieve 2^{n+1} - 1 distinct voltage levels. A generalized structure of an H-bridge multilevel inverter with non-uniform dc levels is illustrated in Fig. 4.

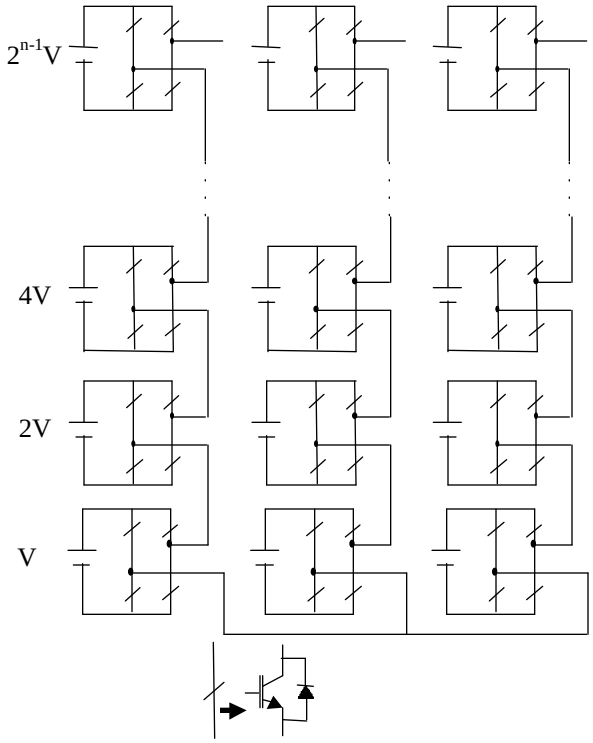

Fig. 4. Simplified schematic of a 2^{n+1} - 1 level H-bridge inverter with n dc voltage levels arranged in binary fashion.

It is interesting to observe a close resemblance of this binary configuration with the process of analog and digital interconversion. As in a digital to analog converter, one can obtain all the combinations of voltages arranged in binary fashion here. For instance, it is possible to obtain 0V, ±1V, ±2V, and ±3V units of voltages (i.e. seven levels) with only two levels (V and 2V) of dc sources. It may be observed that

the conventional H-bridge configuration with identical dc sources would need three such levels. A comparison of this proposed modified H-bridge topology with the existing topologies is presented in Table I. The attributes selected for comparison are required number of main devices (diodes are not included), number of dc buses or capacitors and number of levels obtained at the output waveform. It may be observed that with the same number of devices and dc buses, the proposed configuration offers better performance in terms of levels than the rest of the topologies.

TABLE I
COMPARISON OF TOPOLOGIES FOR MULTILEVEL INVERTERS

Topology	Primary Devices	DC buses (Capacitors)	Levels in the output
Diode Clamped	6N	N	N + 1
Flying Capacitor	6N	3N - 2	N + 1
Conventional H - bridge	12N	3N	2N + 1
Modified H - bridge	12N	3N	$2^{N+1} - 1$

V. PRACTICAL IMPLEMENTATION OF A HYBRID SEVEN-LEVEL INVERTER DRIVE

The modified H-bridge topology offers a distinctive advantage in the number of levels it can generate with a same number of dc sources and power devices when compared to the conventional configuration. However, it may be noted that the stress on the power device in this configuration is proportional to the voltage level it is used. Hence the devices at the higher end of the inverter will be required to have a larger voltage blocking capability than those which are at a lower end. For the 4.5 kV/500 HP induction machine drive system under investigation, it is proposed to use a combination of a GTO inverter with a 3 kV bus and a IGBT inverter with a 1.5 kV bus respectively. It may be observed that, with such a configuration, it is possible to synthesize stepped waveforms with voltage levels –4.5 kV, -3 kV, -1.5 kV, 0, 1.5 kV, 3 kV and 4.5 kV using only six independent dc voltage sources. A simplified schematic of the power circuit of the topology is illustrated in Fig. 6.

As shown in Fig. 6, the higher voltage levels (±3 kV) are synthesized using GTO inverters while the lower voltage levels (±1.5 kV) are synthesized using IGBT inverters. But it is well known that the switching capability of GTO thyristors is limited at higher frequencies [11]. Hence a hybrid modulation strategy which incorporates stepped synthesis in conjunction with variable pulse width of the consecutive steps is proposed. Under this modulation strategy, the GTO inverter is modulated to switch only at fundamental frequency of the inverter output while the IGBT inverter is used to switch at a higher frequency. The proposed static transfer characteristics for the GTO and IGBT switch modulators are illustrated in Figs. 7 and 8.

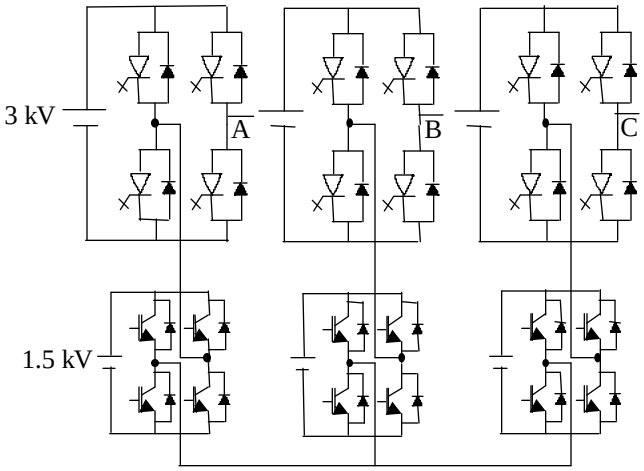

Fig. 6. Simplified schematic of the power circuit of the proposed hybrid seven-level H-bridge inverter.

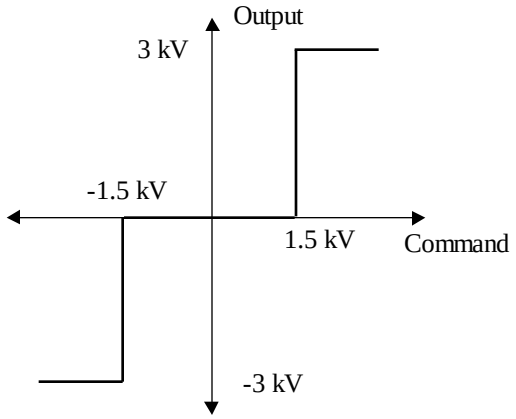

Fig. 7. Static transfer characteristics of the GTO switch modulator.

Fig. 7 illustrates the static transfer characteristics of the GTO modulator. As may be observed from this figure, the GTO inverter is capable of synthesizing a square wave of amplitude 3 kV. This inverter contributes to the output when the command signal is greater than ±1.5 kV (half of ±3 kV). (Please note that the term “command signal” is used to specify the desired output in this paper). If the command is smaller than +1.5 kV, the IGBT inverter synthesizes the pulse width modulated waveform which switches the output between +1.5 kV and 0. The static transfer characteristics of the IGBT inverter are illustrated in Fig. 8. After the command signal crosses +1.5 kV threshold, the IGBT inverter

effectively adds or subtracts 1.5 kV from the +3 kV output synthesized by the GTO inverter. The IGBT inverter is switched between -1.5 kV and 0 until the command signal reaches +3 kV. This effectively subtracts 1.5 kV from the +3 kV synthesized by the GTO inverter. Beyond +3 kV, the IGBT inverter flips between +1.5 kV and 0 thus adding 1.5 kV to the +3 kV generated by the GTO inverter. A similar modulation strategy is applied for negative voltage synthesis. The modulation process and the state of the inverters for various levels of command signals is summarized in Table II.

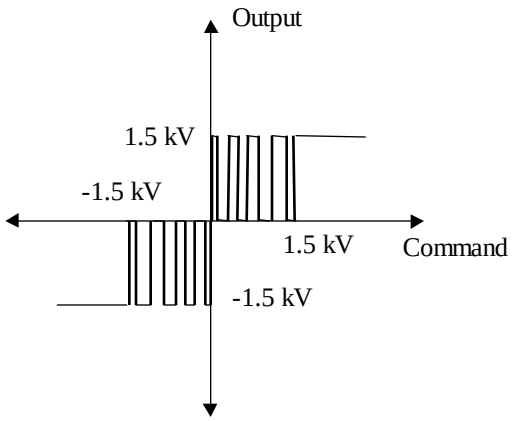

Fig. 8. Static transfer characteristics of the IGBT switch modulator.

TABLE II
MODULATION STRATEGY

Command Signal (Desired Output)	GTO Inverter	IGBT Inverter
Between -4.5 and -3.0 kV	-3 kV	0 ↔ -1.5 kV
Between -3.0 and -1.5 kV	-3 kV	0 ↔ 1.5 kV
Between -1.5 and 0.0 kV	0 kV	0 ↔ -1.5 kV
Between 0.0 and 1.5 kV	0 kV	0 ↔ 1.5 kV
Between 1.5 and 3.0 kV	3 kV	0 ↔ -1.5 kV
Between 3.0 and 4.5 kV	3 kV	0 ↔ 1.5 kV

a ↔ b : Switching between a and b

With this proposed hybrid topology and modulation strategy, the effective spectral response of the output depends on the IGBT switching, while the overall voltage generation is decided by the voltage ratings of the GTO thyristors. This is demonstrated in the illustration of a typical synthesized waveform in the simulation results presented in the following section.

VI. Simulation Results

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level hybrid inverter is constructed in MATLAB-Simulink software. A hybrid modulation strategy which combines fundamental frequency switching for GTO thyristors and open loop PWM control for IGBTs is employed. The schematic of the modulator built in MATLAB-Simulink is illustrated in Fig. 9.

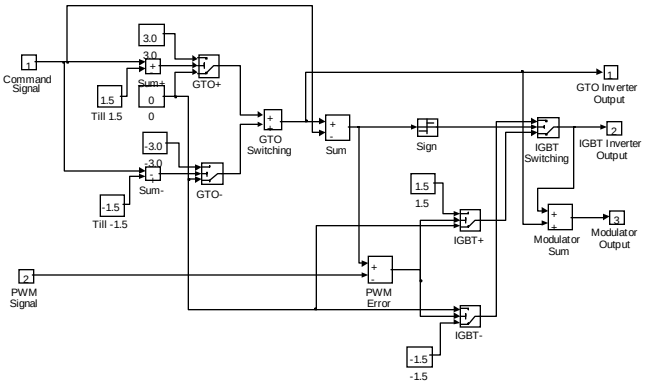

Fig. 9. Schematic of the modulator for the proposed hybrid multilevel inverter.

As shown in Fig. 9, the command signal is compared with a threshold of ±1.5 kV. If it is larger than the threshold, GTO inverter contributes to the output with ±3 kV. The difference between the output of the GTO inverter and the command signal is then compared against a PWM (ramp) signal to modulate the IGBT inverter. The resultant phase voltage obtained from a command signal with modulation index 0.9 is illustrated in Fig. 10. The switching patterns for the GTO thyristors and IGBTs are shown in Figs 11 and 12.

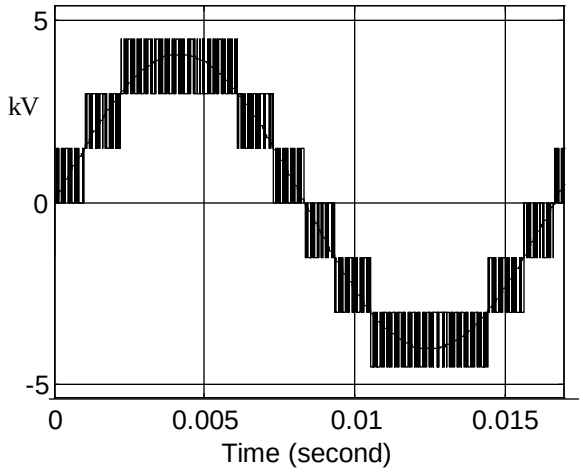

Fig. 10. Typical phase voltage waveform synthesized by the proposed seven-level hybrid inverter.

It may be seen that although the GTO inverter

switching is stepped (Fig. 11), the overall waveform quality is mainly decided by the intermediate IGBT inverter switching (Fig. 12). The GTO inverter participates in synthesizing the required high voltage level while the IGBT inverter acts as a harmonic compensator.

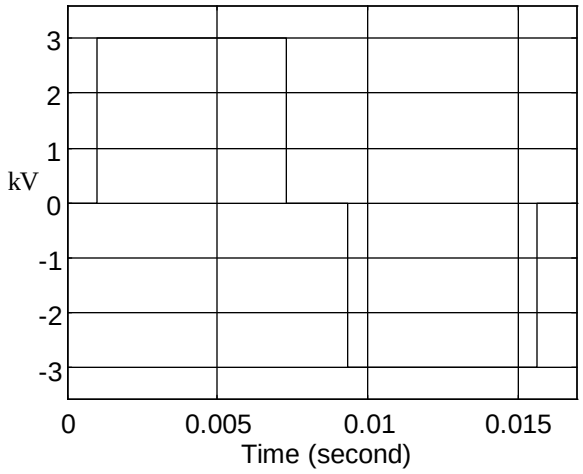

Fig. 11. GTO thyristor switching.

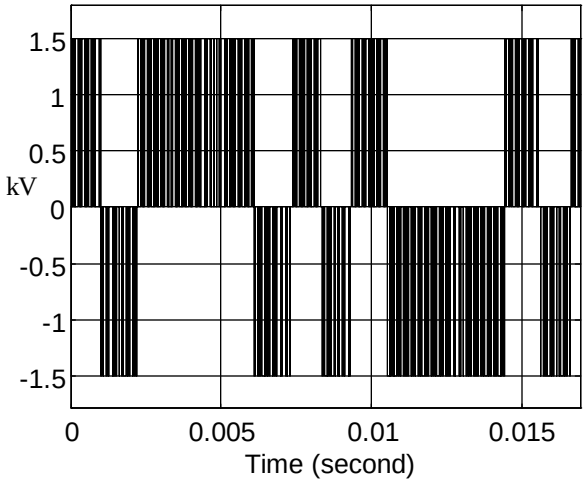

Fig. 12. IGBT switching.

VII. CONCLUSIONS

A hybrid approach for multilevel power conversion has been presented. The proposed topology results from modifying the conventional structure of an H-bridge multilevel inverter. It is demonstrated that by employing non-identical dc voltage sources (particularly a binary arrangement), one can obtain significant increase in the number of synthesized levels. With the proliferation of semiconductor technology, a trade-off has been observed in the selection of power devices in terms of switching frequency and voltage blocking capability. Typically, devices which can switch at faster rates are known to have limited voltage blocking capability and vice versa. This paper has proposed a synergistic approach which combines the fast switching ability of IGBTs and large voltage blocking capability of GTO thyristors. The hybrid multilevel inverter presented in this paper is realized using a combination of a high voltage GTO inverter and a fast switching IGBT inverter. It is shown that the spectral performance is enhanced by the IGBT modulation while a large voltage synthesis is contributed by the GTO inverter. Moreover, this approach enables one to obtain a seven-level conversion with only two dc bus levels. This reduces the cost and effort spent in capacitor voltage balancing. The other significant advantages are that the switch count is lower for same number of levels and the switching losses are curtailed owing to the hybrid modulation strategy.

Finally, a brief comparison of the proposed configuration for seven-level voltage generation with the topologies reported in literature is presented in Table III. It may be observed that the proposed approach offers the same number of levels at the output with a least number of primary devices and dc voltage sources.

TABLE III
COMPARISON OF SEVEN-LEVEL INVERTER TOPOLOGIES

Topology	Primary Devices	DC buses (Capacitors)	Levels in the output
Diode Clamped	36	6	7
Flying Capacitor	36	16	7
Conventional H - bridge	36	9	7
Modified H - bridge	24	6	7

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